SmartVID Controller IP Core User Guide

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2015.12.14

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SmartVID Controller Overview

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The SmartVID Controller IP core enables devices to operate at lower VCC while retaining the same performance level, reducing the overall power consumption.

The SmartVID computing algorithm uses the device speed grade information and targets the operating voltage through fuse values to determine the desired voltage identification (VID) code. The SmartVID Controller IP core then sends the VID code to an external voltage regulator on a parallel interface. For Industrial speed grade, the SmartVID controller takes in additional input from on-die temperature sensor to perform a temperature compensated voltage change operation.

Note: To use the SmartVID controller IP core, you need a device that supports VID operation. VID supported devices have a –V suffix in the device code. Contact your nearest Altera sales representative to access the –V part.

Item		Description
Release Information	Version	15.1
	Release	November 2015
	Product ID	FFFF
IP Core Information	Core Features	• Enables computation delay and computed VID code magnitude adjustment • Lowers voltage according to the temperature obtained from the Temperature Sensor
	Device Family	Supports Arria 10 devices
	Design Tools	• Quartus Prime software for IP design instantiation and compilation • Temperature Sensor IP core

SmartVID Controller Getting Started

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The SmartVID Controller IP core is installed as part of the Quartus® Prime installation process.

Related Information

- **Introduction to Altera IP Cores**
  Provides general information about all Altera IP cores, including parameterizing, generating, upgrading, and simulating IP.
- **Creating Version-Independent IP and Qsys Simulation Scripts**
  Create simulation scripts that do not require manual updates for software or IP version upgrades.
- **Project Management Best Practices**
  Guidelines for efficient management and portability of your project and IP files.

Specifying Parameters and Options

Follow these steps to specify the SmartVID controller parameters and options.

1. Create a Quartus Prime project using the **New Project Wizard** available from the File menu.
2. To enable the SmartVID operation, select a device with VID capability (with OPN-V). You can obtain the -V part device password from your nearest Altera representatives.
3. On the **Tools** menu, click **IP Catalog**.
4. Under **Installed IP**, double-click **Library** > **Low Power** > **SmartVID Controller IP**.
   The parameter editor appears.
5. Specify a top-level name for your custom IP variation. This name identifies the IP core variation files in your project. If prompted, also specify the targeted Altera device family and output file HDL preference. Click **OK**.
6. Specify parameters and options in the SmartVID Controller parameter editor:
   - Specify parameters defining the IP core functionality, and device-specific features.
   - Specify options for processing the IP core files in other EDA tools.
7. Click **Generate** to generate the IP core and supporting files, including simulation models.
8. Click **Close** when file generation completes.
9. Click **Finish**.
10. If you generate the SmartVID Controller instance in a Quartus Prime project, you are prompted to add **Quartus Prime IP File (.qip)** and **Quartus Prime Simulation IP File (.sip)** to the current Quartus Prime project.

SmartVID Controller Parameters

You can use the GUI parameters to configure the SmartVID Controller IP core.

Table 2-1: SmartVID Controller Parameters

The table below lists the options in the SmartVID Controller parameter editor.

Parameters	Value	Description
Device family	Arria 10	This IP core is specifically for Arria 10 devices.
Core Speed Grade	–3, –2, or –1	Select the core fabric speed grade of the FPGA. **Note:** If you select –1, the AVS feature will not be enabled.
Enable AVS Feature	**On** or Off	Turn on this option to enable the Adaptive Voltage Scaling (AVS) feature. **Note:** When you turn on the AVS feature, ensure that `ENABLE_SMART_VOLTAGE_ID` is set to `ON` in the **Quartus Setting File (QSF)**.
Bypass VID Controller configuration register programming	**On** or Off	• Turn on this option to allow the IP core to start operation after it is out of reset. The IP core will start operating immediately based on your settings. • Turn off this option if you do not want the IP core to start operation until the configuration registers are fully programmed.

Note: Advanced users can configure and read the status of the SmartVID IP cores through the configuration registers.

Related Information

SmartVID Controller Configuration Registers on page 5-1

SmartVID Functional Description

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The SmartVID Controller IP core connects to the other sub-systems in a device.

Figure 3-1: SmartVID Controller Block Diagram

The figure below shows a block diagram of the SmartVID Controller IP core.

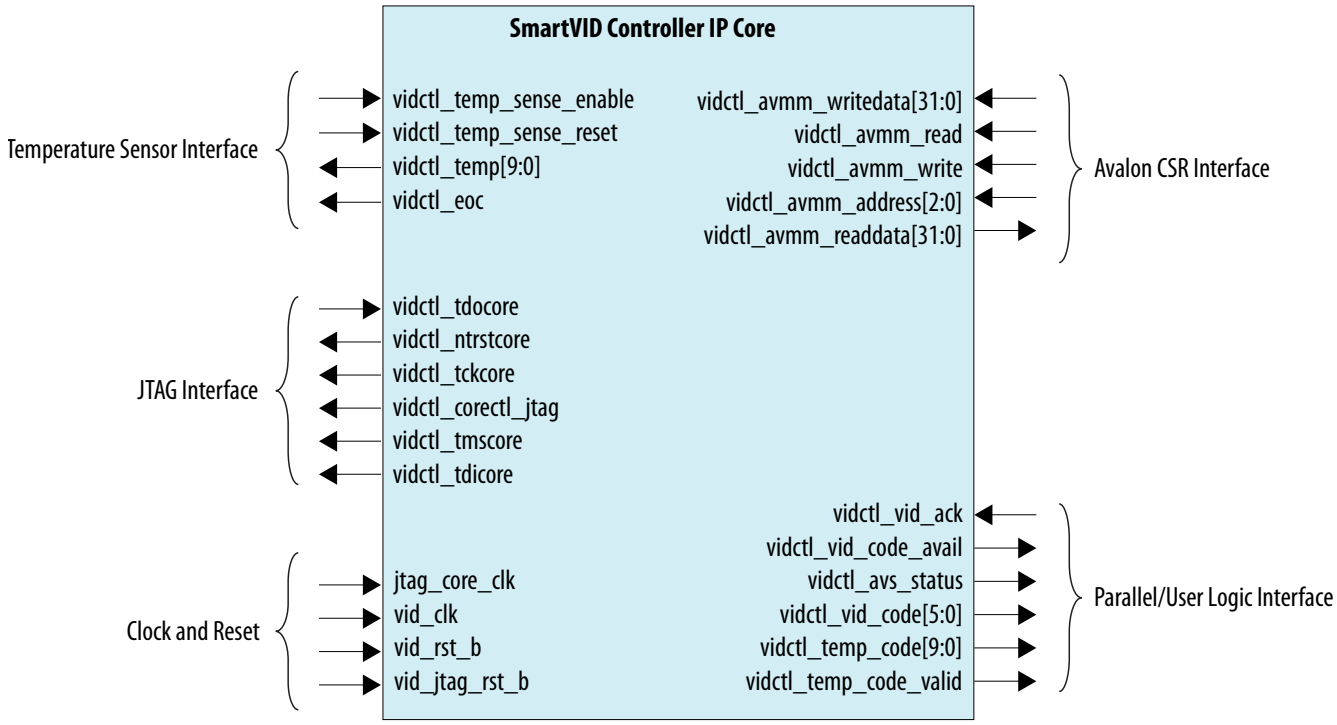


Table 3-1: SmartVID Controller Interfaces

Interface	Description
Clock Reset	• The SmartVID controller requires `vid_clk` at 125 MHz and `jtag_core_clk` at 25 MHz. • Deassert `vid_rst_b` and `vid_jtag_rst_b` after `vid_clk` and `jtag_core_clk` have each toggled for at least 10 clock cycles.

Interface	Description
JTAG	Uses the JTAG interface to retrieve the fuse value from the JTAG atom on an Arria 10 device.
Temperature Sensor	Uses the temperature sensor to sample the temperature code for the SmartVID controller operation.
Avalon Control and Status Register (CSR)	To change the control and status register values on the fly, (for advance users).
User Logic	• To interface with the user logic. • When `vid_code_avail` is high, the user logic controller asserts `vid_ack`.

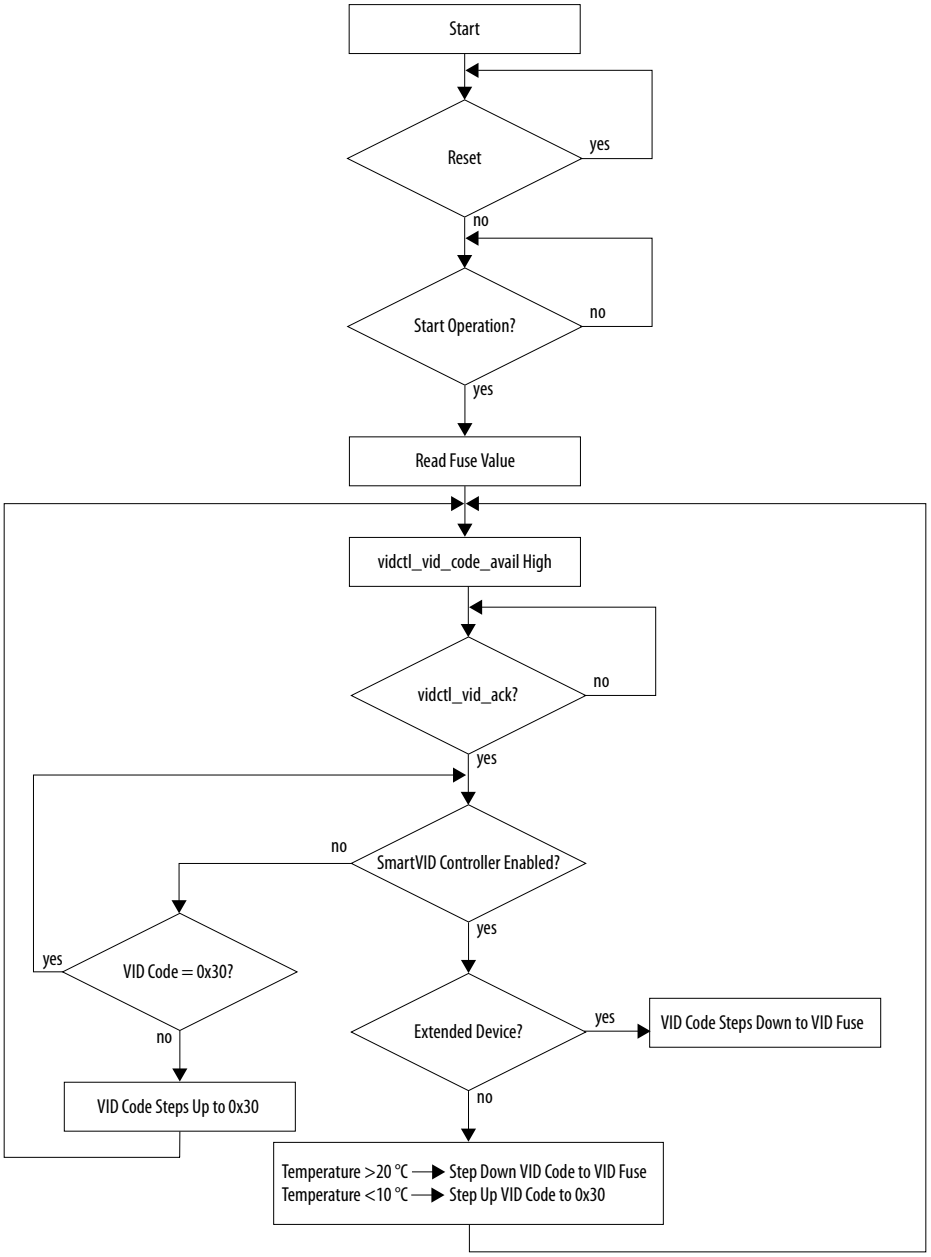
Related Information

- **Temperature Sensor IP Core User Guide**
  Provides more information about the Temperature Sensor IP core.
- **Temperature Value**
  Provides more information about how to calculate the temperature value.
- **Power Management in Arria 10 Devices**
  Provides more information about the JTAG block in Arria 10 devices.

SmartVID Controller Operation

The SmartVID controller operation flow chart shows how the SmartVID controller operates.

Figure 3-2: SmartVID Controller Flow Chart



The following items describe the flowchart sequence.

- When you deassert the reset signal, the SmartVID controller waits for the start operation bit (`VID_OP_START`) or `CC1[0]` register to be 1.
- When `VID_OP_START` or `CC1[0]` register is 1, the SmartVID controller reads the fuse value.
- Then `vidctl_vid_code_avail` goes high indicating a new VID code is available.
- The user logic interface asserts `vid_ack` indicating that the new VID code is read.

- If the SmartVID controller is disabled, the IP core checks if the VID code is 0×30. If the VID code is less than 0×30, the IP core starts incrementing the VID code by *x* value until the default value 0×30 is achieved. Then it waits for the SmartVID controller to be enabled.

  Note: *x* value is 0×10 (10 mv) or the value defined in the `VID_STEP SIZE` register.
- When the SmartVID controller is enabled, the IP core checks if the device temperature grade is Extended (E) or Industrial. If the grade is E, the IP core decrements the VID code by *x* value which causes `vidctl_vid_code_avail` to go high.

  Note: The SmartVID controller is enabled when:

  - `vf1_avs_feature_en` = 1 (read from the fuse)
  - `cc3_smartvid_feature` = 1 (set by turning on **Enable AVS Feature** in the parameter editor)
  - `cc2_dyn_avs_control` = 1 (set through `CC1[0]` register)
- The user logic controller asserts `vid_ack` so that new VID code can be computed. `vid_ack` stays asserted until the VID code achieves 0×30. Every time, when a new VID code is computed, `vidctl_vid_code_avail` goes high. The VID code remains the same until the user logic controller asserts `vid_ack`.

SmartVID Controller Interface Signals

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The SmartVID Controller IP core uses the interface signals to connect with the other sub-systems in the Arria 10 device.

Table 4-1: Input and Output Signals for the SmartVID Controller IP Core

Signal	Direction	Description
vid_clk	Input	Requires 125-MHz clock. Most of the functional blocks in the IP core use this clock.
jtag_core_clk	Input	Requires 25-MHz clock. The fuse-read logic in the IP core uses this clock.
vid_rst_b	Input	An active-low reset synchronized to vid_clk domain. You provide the reset.
vid_jtag_rst_b	Input	An active-low reset synchronized to jtag_core_clk domain. You provide the reset.
vidctl_avmm_writedata[31:0]	Input	Write data from the Avalon-MM Master to the SmartVID controller.
vidctl_avmm_read	Input	Read-transfer indication from the Avalon-MM Master to the SmartVID controller.
vidctl_avmm_write	Input	Write-transfer indication from the Avalon-MM Master to the SmartVID controller.
vidctl_avmm_address[2:0]	Input	The Avalon-MM Master address for data transfer to/from SmartVID controller. This is a word address.
vidctl_avmm_readdata[31:0]	Output	Read data from SmartVID controller to Avalon-MM Master.
vidctl_tdocore	Input	Connect this signal to the tdocore port of the JTAG interface.
vidctl_ntrstcore	Output	Connect this signal to the ntrstcore port of the JTAG atom.
vidctl_tckcore	Output	Connect this signal to the tckcore port of the JTAG atom.

Signal	Direction	Description
vidctl_corectl_jtag	Output	Connect this signal to the corectl port of the JTAG atom. Dynamic FPGA core firewall enable.
vidctl_tmscore	Output	Connect this signal to the tmscore port of the JTAG atom.
vidctl_tdicore	Output	Connect this signal to the tdicore port of the JTAG atom.
vidctl_vid_ack	Input	Your controller should send a pulse to this signal when the vidctl_vid_code signal is sampled and sent to the voltage regulator.
vidctl_temp	Input	Connect this signal to the tempout port of the temperature sensor. This is the temperature code output from temperature sensor.
vidctl_eoc	Input	Connect this signal to the eoc port of the temperature sensor. This is the end of conversion signal from temperature sensor.
vidctl_temp_sense_enable	Output	Connect this signal to the corectl port of the temperature sensor. This is a core enable signal from the core to the temperature sensor.
vidctl_temp_sense_reset	Output	Connect this signal to the reset port of the temperature sensor. This is the reset signal from the core to the temperature sensor.
vidctl_vid_code_avail	Output	Your controller may sample the vid_codewhen this signal is asserted.
vidctl_avs_status	Output	When you assert this signal, the AVS mode is enabled.
vidctl_vid_code	Output	This is a 6-bit VID code from the SmartVID controller.
vidctl_temp_code	Output	This is a 10-bit temperature code from the SmartVID controller.
vidctl_temp_code_valid	Output	This signal indicates whether the vidctl_temp_code value is valid.

SmartVID Controller Configuration Registers

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The control and status configuration registers are meant for advanced users.

The SmartVID Controller IP core uses the Avalon Memory-Mapped (Avalon-MM) interface for read and write operations in a memory-mapped system. The 32-bit non-bursting Avalon-MM slave interface allows upstream to access internal control and status registers.

The SmartVID Controller IP supports a basic one clock cycle transaction bus. Avalon-MM slave interface does not support byte enable access. Avalon-MM slave read and write data width is 32 bits (DWORD access).

Note: The control data is read once at the start of each frame and is buffered inside the IP core, so the registers can be safely updated during the processing of a frame.

Table 5-1: SmartVID Controller Control and Status Register Map

The table below lists the control and status registers for the SmartVID Controller IP core.

Address Offset	Register	Description
0x0	`Capabilities and Control 1 (CC1)`	Configures the capabilities of SmartVID core.
0x1	`Capabilities and Control 2 (CC2)`	
0x2	`Capabilities and Control 3 (CC3)`	
0x3	`VID Fuse1 (VF1)`	Stores VID fuse values [31:0]
0x4	`VID Fuse2 (VF2)`	Stores VID fuse values [63:32]
0x5	`Temperature and Computed VID Codes (TCVC)`	Stores a sampled temperature code, and a computed VID code.

Table 5-2: Capabilities and Control 1 (CC1) Register

Address	Register	RO/RW	Description
31:2	Reserved	RO	This register is reserved for future use.

Address	Register	RO/RW	Description
1	Temperature Sensor Enable	RW	A policy bit that governs whether the temperature sensor of the Arria 10 device is enabled in user mode. • 0: Temperature sensor is disabled. • 1: Temperature sensor is enabled (default). **Note:** The temperature codes from the temperature sensor are also used by other Arria 10 sub-systems. Clear this bit only if enabling the temperature sensor may cause unexpected issues to the Arria 10 device.
0	SmartVID Controller Start Operations (`VID_OP_START`)	RW	A policy bit that determines whether the IP core can start operating when it is out of reset. **Note:** Set this to 1 only after programming all other configuration registers for this IP core.

Table 5-3: Capabilities and Control 2 (CC2) Register

Address	Register	RO/RW	Description
31:27	Reserved	RO	This register is reserved for future use.
26:21	VID Step Size (`VID_STEP`)	RW	These bits determine the final adjustment magnitude of the computed VID code at the end of each computation, if applicable. Each step represents a 5 mV change. Value: 000001 — Adjustment Magnitude: 5 mV (default) Value: 000010 — Adjustment Magnitude: 10 mV Value: 000011 — Adjustment Magnitude: 15 mV
20:1	VID Computation Delay (`VID_COMPUTE_DELAY`)	RW	These bits represent the duration that must elapse (in µs) before a new VID code is computed. The legal range for the delay is 10 ms to 1 second. Ensure that this computation delay is longer than the time required for the following tasks: • The time the user logic or controller takes to complete receiving the VID value, including the retry upon error. • The time the voltage regulator takes to reach the voltage represented by the VID value. **Note:** For optimum system considerations, you are recommended to program this computation delay to 10 ms, 100 ms, or 1 second interval, instead of at µs range. For example, 10 ms (10,000 µs) = 00000010011100010000 (2710h).

Address	Register	RO/RW	Description
0	Dynamic AVS Feature Control (DYN_AVS_CONTROL)	RW	This bit dynamically enables or disables the Adaptive Voltage Scaling (AVS) feature. • 0: AVS feature is disabled. • 1: AVS feature is enabled (default). **Note:** The AVS logic in the SmartVID Controller IP core is only enabled when CC2[0], CC3[3], CC3[16], and VF1[4] bits are set to 1.

Table 5-4: Capabilities and Control 3 (CC3) Register

Address	Register	RO/RW	Description
31:17	Reserved	RO	This register is reserved for future use.
16	Device Supports AVS Feature (DEVICE_SUPPORTS_AVS)	RO	This policy bit determines if the AVS feature of the SmartVID Controller IP core can be enabled. • 0: AVS feature is not supported. • 1: AVS feature is supported.
15:10	Live VID Code (VID_DEFAULT)	RO	This bit indicates the live VID code produced by the SmartVID Controller IP core. This live code may be in either static voltage scaling (SVS) or AVS mode.
9:4	Default VID Value (VID_DEFAULT)	RO	These bits indicate the default VID value.
3	AVS Feature Enable (AVS_ENABLE)	RO	This policy bit determines if the AVS feature of the SmartVID Controller IP core can be enabled. **Note:** The AVS logic in the SmartVID Controller IP core is only enabled when CC2[0], CC3[3], CC3[16], and VF1[4] bits are set to 1.
2:1	Core Speed Grade (CORE_SPEED_GRADE)	RO	These bits indicate the core fabric speed grade of the FPGA device. Bits / Speed Grade: 00 → –3; 11 → –2; 10 → –1; 01 → Reserved
0	Reserved	RO	This register is reserved for future use.

Table 5-5: VID Fuse1 (VF1) Register

Address	Register	RO/RW	Description
31	Reserved	RO	This register is reserved for future use.

Address	Register	RO/RW	Description
30	VID Fuses Valid	RO	This bit indicates whether the non-reserved fields of this register have valid values or not. • 0: Values of non-reserved fields of this register are invalid. • 1: Values of non-reserved fields of this register are valid.
29:24	VID For Dash –1 Core Speed Grade	RO	These bits are mapped to the retrieved `VID Fuse[29:24]`, which represent the VID code for –1 core speed grade. Refer to **VID Codes for Arria 10 Speed Grades** on page 5-5.
23:22	Reserved	RO	This register is reserved for future use.
21:16	VID For Dash –2 Core Speed Grade	RO	These bits are mapped to the retrieved `VID Fuse[21:16]`, which represent the VID code for –2 core speed grade. Refer to **VID Codes for Arria 10 Speed Grades** on page 5-5.
15:14	Reserved	RO	This register is reserved for future use.
13:8	VID For Dash –3 Core Speed Grade	RO	These bits are mapped to the retrieved `VID Fuse[13:8]`, which represent the VID code for –3 core speed grade. Refer to **VID Codes for Arria 10 Speed Grades** on page 5-5.
7:5	Reserved	RO	This register is reserved for future use.
4	AVS Feature Enable Via Fuse	RO	This bit is mapped to the retrieved `VID Fuse[4]`, which determines if the AVS feature of the SmartVID Controller IP core can be supported. • 0: AVS feature is not supported. • 1: AVS feature is supported. **Note:** The AVS logic in the SmartVID Controller IP core is only enabled when `CC2[0]`, `CC3[3]`, `CC3[16]`, and `VF1[4]` bits are set to 1.
3:0	Reserved	RO	This register is reserved for future use.

Table 5-6: Temperature and Computed VID Codes (TCVC) Register

Address	Register	RO/RW	Description
31:28	Reserved	RO	This register is reserved for future use.
27	AVS Status	RO	This bit indicates the operating state of the SmartVID Controller IP core AVS logic. • 0: AVS logic is deactivated. • 1: AVS logic is active.

Address	Register	RO/RW	Description
26:17	Temperature Used In AVS VID Computation	RO	These bits capture the temperature code used in the latest computed VID code when AVS logic is active. This information is intended for correlation and debugging purposes. **Note:** These bits are set to 0 if `CC1[1]` and `CC1[2]` bits are 0 and the AVS logic is deactivated.
16	Temperature Code Valid	RO	This bit indicates whether TCVC[9:0] has a valid temperature code. • 0: `TCVC[9:0]` value is invalid. • 1: `TCVC[9:0]` value is valid. **Note:** This bit is set to 0 if `CC1[1]` is 0.
15:10	Latest Computed VID Code in AVS mode	RO	These bits indicate the latest computed VID code when AVS logic is active. When AVS logic is deactivated, these bits will be set to 0.
9:0	Temperature Code	RO	These bits indicate the periodically sampled temperature code output by the temperature sensor. **Note:** These bits are set to 0 if `CC1[1]` is 0.

VID Codes for Arria 10 Speed Grades

You can derive the VID codes for the different speed grades using this formula:

```
Voltage = (VID Code–28)×0.005V+0.8V
```

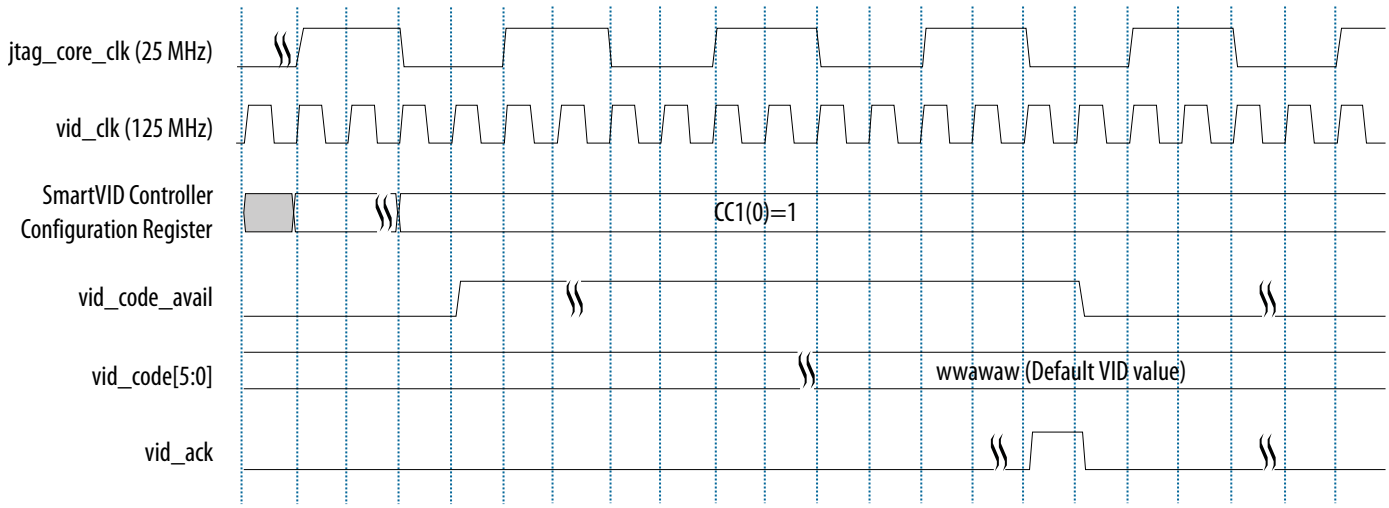
Table 5-7: Example VID Codes for Arria 10 Speed Grades

VID Code (Binary)	Voltage (V)
011100	0.800
011101	0.805
011110	0.810
...	...
101111	0.895
110000	0.900
110001	0.905
...	...
111101	0.965
111110	0.970
111111	0.975

System Power-On

The figure shows the state of operation of the SmartVID controller IP core during system power-on with the relevant Arria 10 sub-systems.

Figure 5-1: Operation Behavior



When the `CC1[0]` register is 1, the IP core initiates VID fuse-read. The SmartVID Controller IP core then switches to AVS mode when the following conditions are met:

- SmartVID (AVS) logic enabled.
- The external controller reads out the default VID value and asserts `vidctl_vid_ack`.
- The duration specified in the `CC2[20:1]` register elapses.

SmartVID Controller Reference Design

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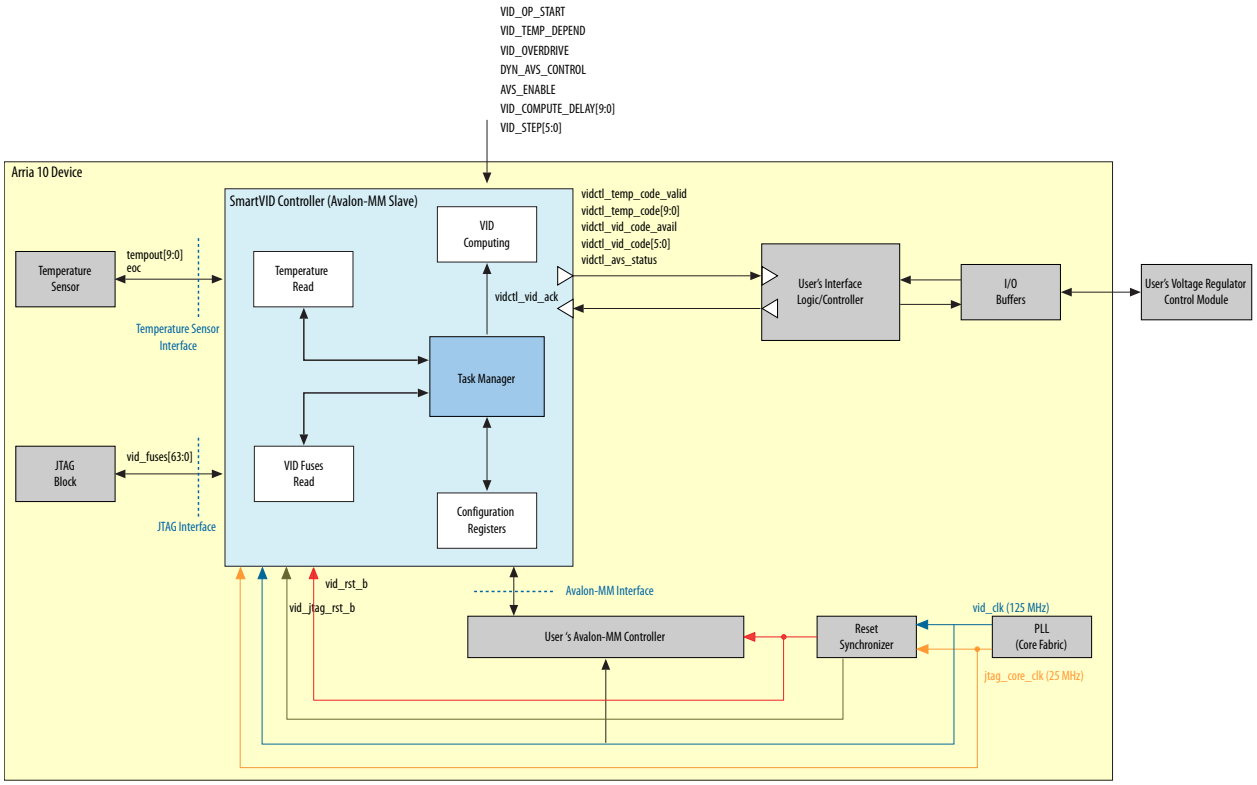
The SmartVID Controller reference design provides you an overview of the SmartVID controller system.

Figure 6-1: SmartVID Controller System with Arria 10 Device

The figure below shows the system-level block diagram of the SmartVID controller with the interfacing sub-systems within an Arria 10 device.



The SmartVID controller reference design contains the following components:

- Reset synchronizer
- Voltage regulator
  - Designed to remap the VID code from the SmartVID controller IP core to the corresponding voltage code of the targeted voltage regulator. After 1 clock cycle, `vidctl_vid_code_avail` goes high and the voltage regulator reads the VID code and asserts `vid_ack`.
- Temperature sensor
- JTAG block
- IOPLL
  - The design uses the IOPLL to provide the 125-MHz and 25-MHz clocks when the board does not have a particular clock source.

Related Information

SmartVID Controller Reference Design
Click to download the design file.

Document Revision History for SmartVID Controller User Guide

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Date	Version	Changes
December 2015	2015.12.14	• Added information about how to obtain the password for the device code. • Added detailed description about the SmartVID controller block diagram. • Added a flow chart and detailed description of how the SmartVID controller operates. • Updated the configuration registers. These registers are meant for advanced users. • Provided link to SmartVID controller reference design.
May 2015	2015.05.04	Updated the legal range for the VID Computation Delay (`VID_COMPUTE_DELAY`) register from 1 ms–1 second to 10 ms–1 second.
December 2014	2014.12.15	Initial release.

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