Thermal Solutions for 3-D IC, Packages and System

For many 3-D IC design applications, thermal management is critical, since accurate temperature maps can impact a chip's reliability and performance including electromigration (EM) limits, voltage (I^2R) maps and power distribution. The chip, package, board and system are all thermally coupled, but in different length scales, such as um, mm and hundreds of mm.

Many chip thermal behavior studies [1, 2, 3 4, 5] oversimplify thermal boundary conditions surrounding a single chip: namely, equivalent heat transfer coefficient on the top face of a chip for heat sink effects and assumed adiabatic or user-defined thermal boundary conditions on the other five faces. These simplified thermal boundary conditions are difficult to justify, especially for multiple chips in system-in-package (SiP) or 3-D IC designs. As demonstrated in the literature [6], different designs of packages and modeling details have a big impact on thermal responses on chips, and this must be addressed properly in thermal modeling. In addition, the variations of a system thermal environment outside the package can have a big impact on chip thermal responses, so these should be considered in analysis.

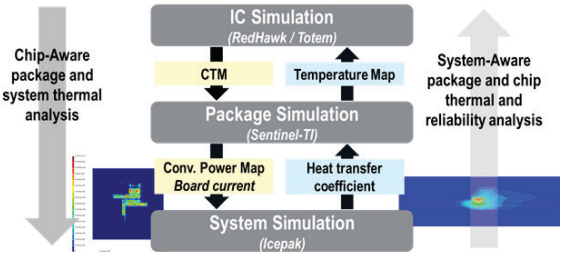

Figure 1. ANSYS Apache chip–package–system thermal solution

It is a challenge to include details for all levels of thermal coupling in one analysis model using current technology, as the model size could be excessively large. An accurate coanalysis flow methodology [6] is proposed to help manage thermal problems in 3-D ICs for chips in package on board configurations using a submodeling approach. Chip models at micron level serve as the submodel of a package/board model in mm scale, through a work flow for chip and package tools, for power and thermal calculations. The study in this paper extends the cowork scope further to chips/package in a system, which may include a more-complex board with multiple heating components or boards enclosed in a box or case, with blowers and grilles. The system model includes airflows inside the application box using computational fluid dynamics (CFD) technology. The chip-in-package is the submodel in the system. This hierarchical modeling methodology and the cowork flow in chip–package–system have a minimum of simplifications and assumptions. They cover the thermal analysis needs for most realistic scenarios in any electronic application with sufficient details.

For temperature-dependent chip power, a chip thermal model (CTM)-based thermal analysis is proposed to predict converged temperature and power on 3-D IC chips using a system thermal environment (Figure 1). CTM is a library of temperature-dependent power and per-metal layer density information of a chip for use in chip–package thermal analysis. The results of this thermal analysis are useful for temperature-aware chip EM reliability, IR drop and power calculations for chip sign-off. A CTM is associated with a particular chip activity mode, for example viewing video or talking on a smart phone. The temperature ramp for a series of chip activities can be predicted once the thermal results from CTM analyses are available.

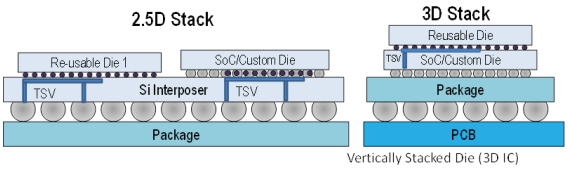

Figure 2. Popular 2.5-D (left) and 3-D IC (right) package designs [8,9]

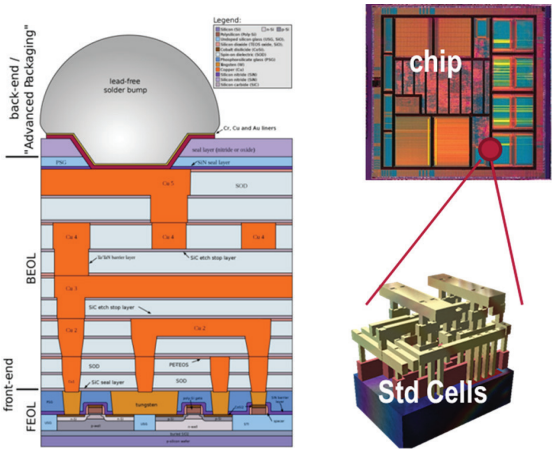

Figure 3. Schematic structure of CMOS chip [10] and its 3-D structure [11] of standard cell

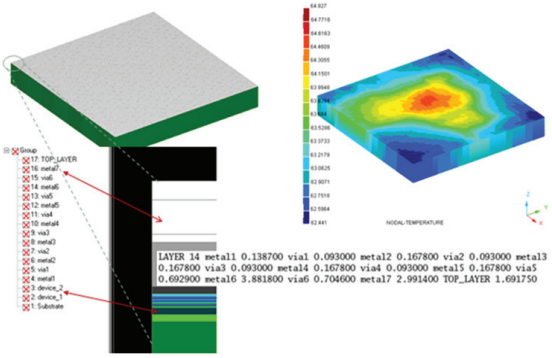

Figure 4. Typical chip thermal model with multi-layer structure on thin layers on top of silicon chip along with temperature profile with model resolution in microns.

This approach can also be used to study power mode switching in a chip to control the temperature limit.

This paper reviews the important elements in 3-D IC thermal prediction: generating a power (T) library for chips, and thermal modeling from chip, package, to system, along with cowork among thermal tools at different levels. It presents CTM-based task flows; background of temperature dependency in chip power; case studies of CTM-based analysis, including thermal back-annotation, multi-activity chip thermal transients, system thermal improvements to reduce chip temperature, and effects of self-heating on board to chip temperature.

Key Elements in 3-D IC Thermal Modeling and Analysis

Current 3-D IC package designs feature stacked dies with microbumps and through silicon via (TSV) connections. The 2.5-D and 3-D IC configurations shown in Figure 2 are popular. For 2.5-D IC design, active dies are connected through microbumps to a silicon interposer (passive die), which redistributes electrical connections through TSVs to C4 bumps mounted on a BGA substrate. Active die can be realized using existing 2-D IC design technology, and the cost of a passive silicon interposer with TSVs is less than that of an active die with TSVs. Using silicon interposer is the most practical 3-D IC integration method today. True 3-D IC designs need to embed TSVs in the active die, which is more expensive in design and fabrication but will become practical in years to come [7]. Die stacking in 3-D ICs is not limited to two; it can include many dies stacked together. With closely stacked die in 3-D IC packages, thermal management is critical.

Chip structure is of a 3-D nature, even for conventional 2-D design. Figure 3 shows layers of a cut-section of a CMOS chip and 3-D structure in a standard cell, which is the basic logic function unit. There can be millions of basic units on a chip. From a thermal analysis viewpoint, it is desirable to have an analysis model reflect the true thermal conductivity of all the details. In practice, simplifications and assumptions must be used in constructing a chip thermal model with good accuracy.

Figure 4 shows an example of a chip thermal analysis model with a multi-layer structure on thin layers on top of a silicon chip. The expected temperature profile of the whole chip reflects the patterns of power maps on chip layers as well as the thermal conductivity distribution on layers. The thermal gradient on-chip can be as small as a few degrees in Celsius in low-power applications with good packaging and a cool system environment. For high-power applications, the thermal gradient on-chip can be more than a dozen degrees Celsius. There can also be thermal gradients among the layers, as shown in Figure 5. In the case of 3-D ICs, the active die with TSVs has back metal layers on the chip side, opposite of the main heating surfaces. The existence of TSVs and back metal layers affects the thermal profile of the chip, due to thermal conductivity distribution differences. The most useful thermal result for a chip designer is the converged layer-aware thermal profile. The thermal profile of the chip affects the local EM prediction, which in turn affects the reliability of the chip. Typically, the higher the temperature, the lower the EM limit, or reliability in the local area of

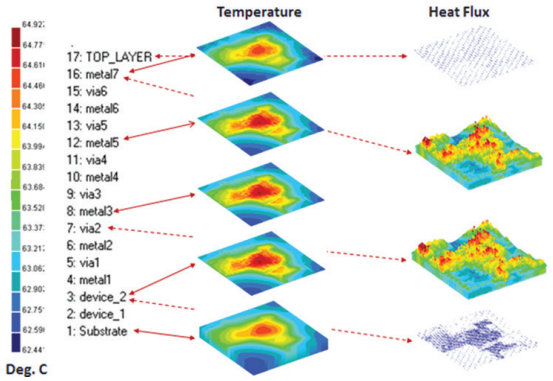

Figure 5. Thermal gradient across layers in a chip along with heat fluxes showing how heat flows through layers

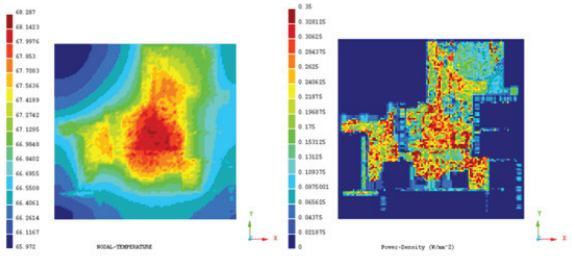

Figure 6. Temperature and power profiles on CMOS device layer in chip

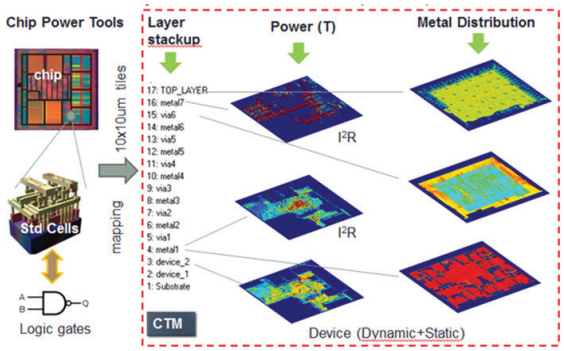

Figure 7. 3-D distribution of temperature-dependent power map for chip. A CTM is a tile-based power library at uniform temperature points, which provides complete temperature-dependent power information and tile-based metal distribution for use in chip–package thermal analysis.

the chip. Figure 6 shows the converged thermal profile and the corresponding power map with matching hot spots. Convergence through iterations is needed as power is temperature-dependent. This process is explained in the following sections.

Thermal profiles are the responses from die power and its thermal boundary conditions. Power in a chip is also 3-D in nature, and it is associated with chip layers — that is, CMOS device layer for dynamic and static power, and interconnection layers for self-heating power. The CTM in Figure 7 is a tile-based power library at uniform temperature points, which provide complete temperature-dependent power information and metal distribution for use in chip thermal analysis. The thermal profiles in Figures 4, 5 and 6 are based on power maps in a CTM.

A package provides the direct heat dissipation paths from the chips to a system. Since the package is adjacent to the chips, sufficient details of the package must be included in a thermal model for accurate chip thermal responses. Thermal couplings among chips in a 3-D IC package are included if the package is properly modeled. A previous study [6] shows that in some cases, small details such as microbump distribution and metal traces/vias will have an impact on chip thermal responses, up to 20 percent changes in temperature rise per watts. Figure 8 shows a 3-D IC example of die placements in a package.

The package alone cannot dissipate enough heat to cool the chips. A package must be mounted on the PCB, and the PCB is typically mounted in a box with other heating components, such as batteries, and with fans to force air cool-down of the chips (Figure 9). If this is still not enough, a heat sink can be attached to top of the package to help dissipate heat directly from the die (Figure 8). The configuration in Figure 9 needs CFD technology to simulate airflow, which is crucial to heat dissipation in the system.

Throughout this paper, Figures 2 through 9 describe the key components in chip thermal simulation for 3-D IC — chip, package and system. Chip power generation, chip and package thermal modeling, and system environment (coanalyses of chip, package and system) tools are needed for accurate chip thermal simulation. The flow diagram in Figure 10 illustrates coanalyses steps.

1. Chip power tools from Apache, RedHawk™ [12] and/or Totem™ [13], are used for CTM generation. RedHawk is used for logic and analog die.

2. The CTM library per chip is passed to the chip thermal tool, Apache's Sentinel™-TI [14], which has detailed package components surrounding the 3-D IC in its analysis model. To start the analysis flow, Sentinel-TI attaches a PCB to the package to generate a complete heat dissipation system and perform a CTM-based thermal analysis to generate converged temperature and power maps. (When thermal BCs from step 3 are available after the first iteration, Sentinel-TI wraps the package-only model with system thermal BCs to update thermal results.) The chip thermal models are layer-aware, and the power maps are formed by

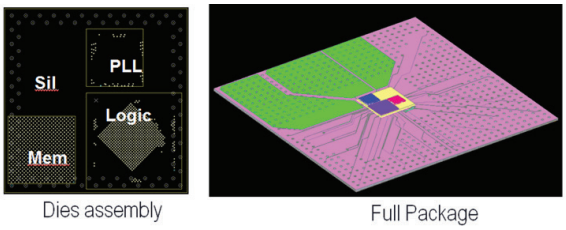

Figure 8. Chips in package, with 2-D designs for memory, logic and PLL as well as TSVs in silicon interposer, which is 3-D IC configuration

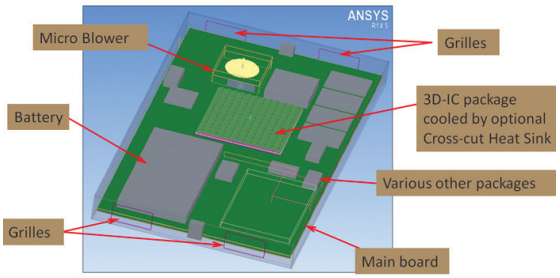

Figure 9. 3-D IC package in system enclosed by box (hand-held device)

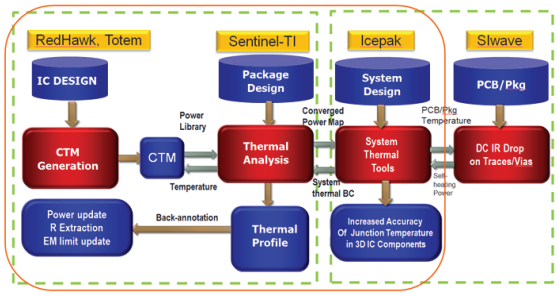

Figure 10. Coanalysis flow diagram in ANSYS tools for chip thermal integrity with system thermal environment. For this paper, the focus is on coanalysis (red box). On the left, the green box shows the cowork of chip power and chip–package thermal tools from ANSYS and Apache, and the green box on the right shows ANSYS tools for system thermal and package–PCB DC self-heating for additional accuracy.

small power tiles, for example 10 um x 10 um. The power tiles on one die layer (for example, the device layer can be up to 1 million for a 10 mm x 10 mm die with 10 um x 10 um tiles). For self-heating power on interconnection layers, the number of power tiles will multiply and can add up to 10 million for 10 metal/via layers on one chip. The detailed power map captures realistic thermal responses in each die on the layers. Iterations in Sentinel-TI are needed to reach temperature and power convergence for each die in the package/PCB environment.

3. For system thermal BCs, the converged power map of the Sentinel-TI run is reduced to less than a couple thousands of heating objects per die and passed to ANSYS® Icepak®, which models simplified silicon blocks as chips in 3-D IC design. Icepak is a CFD tool that models silicon blocks in a package mounted on a PCB in a system with airflow inside a box. Complex airflows in and out of the box are simulated for realistic system thermal responses. The thermal boundary conditions surrounding the package can be extracted after the CFD analysis for use by the chip–package model in Sentinel-TI.

4. Returning to step 2 above, the system thermal boundary conditions for the package from CFD analysis feed back to Sentinel-TI for a chip–package-only model to rerun the CTM-based thermal analysis and generate new reduced-power maps for the Icepak CFD model.

5. Repeat steps 3 and 4 until the temperature and power are converged in Icepak, or the temperature and power in Sentinel-TI remains unchanged. Move next to step 6 for thermal back-annotation to chip design.

6. RedHawk or Totem receives the multi-layer chip thermal profile file for each chip and reruns the EM, IR drop or power analysis for temperature-aware solutions.

If current densities at C4 bumps are available from the chip power calculation, DC IR drop analysis in ANSYS SIwave™ can generate self-heating on traces and vias in package and on PCB (Figure 10). This is a secondary heating effect compared to die heating; however, the self-heating power in a package or PCB can feed back to Icepak as part of the system heating, affecting the chip thermal results.

Temperature Dependency of Chip Power

The key feature in a CTM is the temperature dependency of chip power. Total power in a chip can be divided into dynamic and static parts. Dynamic power is related to the functions of devices in a chip; this was dominant in older chip designs. However, the portion of static power is catching up as technology scales, due to the drive for low power in new chip designs, especially for mobile applications. Static power can be represented by the product of voltage drop and junction leakage current in a CMOS gate:

$$P_{static} \sim V_{CC} * I_{leak}$$

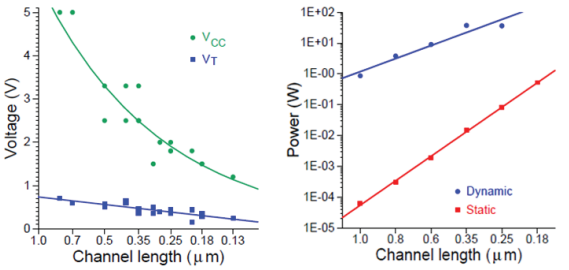

Figure 11. Trend of subthreshold voltage and static (leakage) power; a significant portion is in total power

When technology scales for dimension reduction to increase performance and density, Vcc is reduced to limit dynamic power and electric fields that require lower VT (subshreshold voltage) to maintain sufficient gate override, i.e., V_{cc} - V_T. Figure 11 shows the trend of V_{cc}, V_T, and power [17]. The lower the VT, the easier leakage is in a CMOS gate. Leakage increases exponentially with the drop of V_T:

$$P_{static} \sim \exp(-V_T)$$

Since temperature has the effect of reducing VT on a CMOS device, for example about -4 mV/°C to -2 mV/°C [18], P_{static} will, in general, increase exponentially with the temperature, which can lead to a severe condition in thermal management.

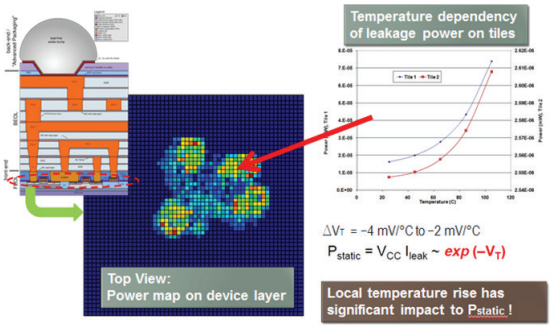

Figure 12. Power including leakage on the device layer is represented in a tile-based map. The leakage part of power on each tile has temperature dependency.

Leakage power on a device layer has 2-D spatial distribution. If dividing a chip into small tiles and calculating the power in the tiles at a given uniform temperature, a power map (Figure 12) is available at the temperature. For several temperature points covering the range of possible die temperatures (for example, 25C to 125C), a set of tile-based power maps is available. The power map for distributed temperature on a chip can easily be calculated through temperature point interpolation, tile by tile. CTM is a collection of power maps with uniform temperature in chip at a few temperature points, typically five. The CTM also includes a self-heating power map and metal distribution for each interconnection layer. Self-heating power (I^2R) is linearly temperature-dependent, due to electrical resistivity (R) of metal wire used in the calculation. The CTM is exported from the chip power tool for use by the chip thermal tool.

Figure 13 shows the thermal convergence process through iterations in CTM-based thermal analysis. The need for iteration is due to temperature dependency of power in all tiles. The plot is for the maximum temperature and total power on a chip. The leveling-off of the temperature and power curves is a good indicator that the power map is consistent with the temperature map. This is called the convergence state in this paper. Figure 14 shows the power and temperature map updates in an iterative process involving the CTM.

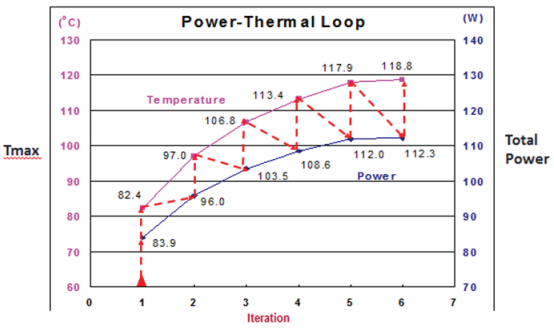

Figure 13. Temperature and power convergence through iterations

Case Studies of CTM-Based Thermal Analysis

Back-Annotation for Chips-on-Silicon-Interposer Design

This study focused on 3-D IC modeling capability and CTM-based thermal analysis. There are coworks between chip–power and chip–package thermal tools. A high-leakage CTM for the logic die was used in the through silicon interposer stack design (Figure 8). The package was mounted on a standard thermal board with still air. The ambient temperatures in the study were 50C and 100C, to reflect the system thermal environment differences. For the three chips in the package (in this example, logic, memory and PLL), the power in the logic die (2.72 mm x 2.72 mm , 65LP) is dominant and is around 0.131W at 25C. With high leakage, the total power in the logic die has more than tripled to 0.48W at 125C (Figure 15). The memory die (2.12 mm x 2.12 mm, 40LP) has low leakage and the total power is only 0.005W. The PLL die is assumed to have negligible power.

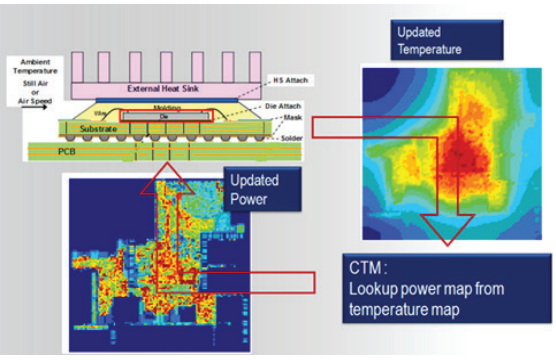

Figure 14. Schematic of power (P) and temperature (T) update loop

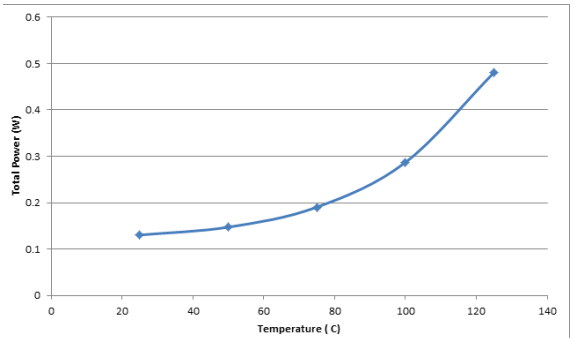

Figure 15. CTM power for logic die with high leakage

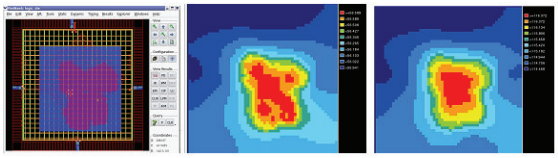

Figure 16. Thermal back-annotation in chip power tool. The left picture is the chip design view from RedHawk. The other two are the temperature contours on the logic chip at an ambient temperature of 50C and 100C, respectively.

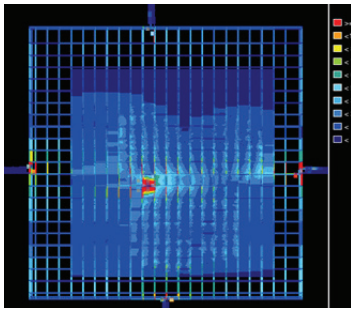

Figure 17. EM map for 100C ambient condition showing a few local regions exceeding the EM tolerance limit of 100 percent

After CTM-based thermal analysis, the layer-aware chip thermal profiles feed back to the chip power tool for recalculation of power, resistance extraction, EM and IR. Figure 16 shows the chip design and thermal profiles in RedHawk for the two system thermal conditions. The temperature gradient is not significant, as this is a small chip, and the power localization is not so significant. The maximum temperature rises above ambient on the logic die are about 6C and 16C for 50C and 100C ambient, respectively. A higher temperature rise at 100C ambient is due to leakage power effects.

For the logic chip, only a very localized region for 100C ambient is seeing EM failure, as in Figure 17. Figure 18 compares the EM map showing the percentage exceeding a fixed tolerance. A 10 percent EM tolerance was used to show the differences due to the temperature level and distribution: from left to right for 100C uniform temperature on chip, 50C and 100C system ambient. Figure 19 shows the IR drop maps on chip at different thermal conditions. Both maximum levels and distributions in IR drop are different due to the thermal distribution differences.

Chip–Package–System Thermal Convergence Study

The system thermal environment (Figure 9) can be more complex than the package on board configuration in the previous study. High-power CTMs are used to study how the system environment can be improved to reduce the chip temperature effectively. The 3D- IC package is the same as in Figure 8. Compared to the previous case, the total power in the logic die was raised to 10x. The high leakage behavior remained the same as in the previous case. The memory chip still had low leakage but a higher total CTM power, around 1.287W. The power for PLL die remained negligible. The ambient temperature outside the box was set to 50C.

The thermal cowork loop occurs between Sentinel-TI and Icepak, as shown in Figure 20. The loops start with a Sentinel-TI CTM-based thermal analysis, with assumed high heat dissipation on the top of the package for powerful heat sink effects. The expected die temperature rise from the ambient is low due to the forced heat dissipation on die tops. The reduced power map after thermal convergence in Sentinel-TI is used by Icepak to generate thermal BC for the package model of Sentinel-TI, with both the heat sink on package top and micro-blower (fan) in the box (Figure 9). The loops between Sentinel-TI and Icepak continue until the maximum temperature changes on the logic die in both tools and remains 5 percent. Figure 21 shows the temperature changes on the logic die through the iterations. The die temperature converged fast, to within 5 percent differences in two loops. The minor differences in die temperature at the convergence from Icepak and Sentinel-TI are due to thermal model differences in the tools. The thermal conductivity distribution in the package may differ between the two tools due to modeling scheme differences. The use of thermal BCs from Icepak in Sentinel-TI also uses approximations and simplifications, such as constant heat transfer coefficients on package sides and top. The power map used in Icepak has been reduced from the detailed multi-layer power map, which may have contributed to chip temperature differences.

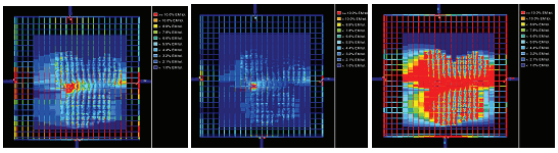

Figure 18. EM map plotted at the 10 percent EM tolerance maximum, showing differences due to temperature level and distribution; left to right: 100C uniform temperature on chip, 50C, and 100C system ambient

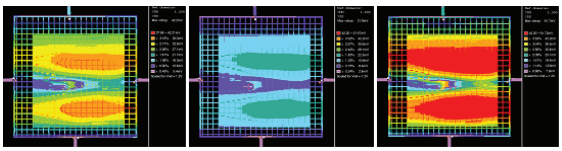

Figure 19. IR map for wire and via with the same maximum voltage drop level (42.2mV); left to right: 100C uniform temperature on chip, 50C, and 100C system ambient

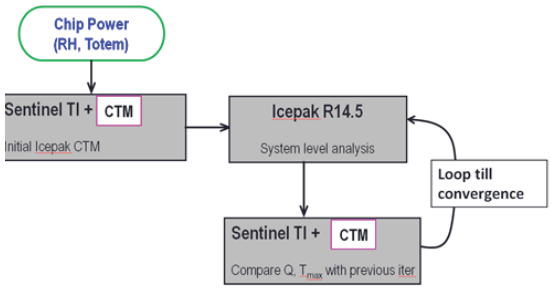

Figure 20. Thermal cowork between Sentinel-TI and Icepak

	Icepak System Thermal	Sentinel-TI Chip Thermal			
		Logic die power (W)		Logic die temperature (C)	
Loop		Power	%Change	T_{max}	%Change
0		*2.43731*		*66.7*	
1	Loop 0 power => Loop 1 BC	2.56834	5.38	98.7	191.62
2	Loop 1 power => Loop 2 BC	2.57157	0.13	99.3	1.23

Figure 21. Loops to temperature convergence of cowork between Icepak and Sentinel-TI

Design Scenarios				Icepak System Thermal	Sentinel-TI Chip Thermal			
					Logic die power (W)		Logic die temperature (C)	
#	Heat sink	Fan	Loop		Power	%Change	T_{max}	%Change
			0		*2.43731*		*66.7*	
1	1	1	1	Loop 0 power => Loop 1 BC	2.56834	5.38	98.7	191.62
2	1	0	1	Loop 0 power => Loop 1 BC	2.64565	8.55	112.3	273.05
3	0	1	1	Loop 0 power => Loop 1 BC	2.5853	6.07	101.8	210.18
4	0	0	1	Loop 0 power => Loop 1 BC	2.75248	12.93	124.3	344.91

Figure 22. Scenarios of system condition changes

There are three other system thermal scenarios studied, as shown in Figure 22. Scenario 1 is described in Figure 21, with both heat sink and fan included. Scenario 2 depicts when the fan failed. Scenario 3 is for the case without a heat sink but with a fan. Scenario 4 is for a bare die case, in which the temperature on chip may exceed the thermal limit at 125C. Scenario 3 is the more attactive due to low cost.

Multi-Activity Thermal Transients

A CTM-based thermal analysis is useful for thermal transient prediction. One application is an electronic device operating at different modes, depending on what the users are doing with it. For example, a smart phone can be used for checking emails or watching YouTube videos. The power consumed or the heat generated will be different. The temperature will be different for reading emails for 10 minutes and watching videos for 8 minutes. In another application, a high-performance operation in a device may require more power, leading to a higher temperature. To avoid overheating, one solution is to have power management in the device, switching to low-power and performance modes when the device temperature reaches a certain limit. This requires thermal transient prediction capability in a design.

The CTM was generated for a user-defined operating mode or activity. There can be multiple activities or CTMs for a chip in different usage modes. The solution for a multi-activity thermal transient is to use the time-to-steady-state curves from the CTM-based thermal analysis for different activities at different locations on a chip.

Consider that a converged power map is switched on at time zero. The temperature map on a chip in a package will gradually build up to its steady state (Figure 23). At each location of interest, there is a temperature rise curve. The rate of temperature rise depends on the thermal resistance of the chip in package on board configuration and the thermal capacitance of the associated materials, such as an RC network in electrical problem. For a series of activities, the power map on and off has the corresponding temperature grow and decay processes (Figure 24). The temporal combination of the temperature transients for each power map or chip activity will provide a good prediction of the overall temperature variations in time. Figure 25 is the transient response at two locations on chip due to two power activities (CTMs) of 10 seconds long each, and repeating 10 times, up to 400 seconds. Figure 26 is the transient response at two locations on chip due to two power activities (CTMs) of 100 seconds long each, and repeating twice, up to 400 seconds.

Self-Heating Effects to Chip Thermal Responses

The flow diagram in Figure 10 shows the coupling between Icepak and SIwave for self-heating in the package or on board. Figure 27 shows the effect of board self-heating affecting chip temperature for a 3-D IC package with two flip chips on a silicon interposer with TSVs using currents from C4 bumps under the silicon interposer [19]. Though self-heating is generally negligible in chip-package analysis as die power is dominant in the package, there is a 7.5 percent temperature rise on the chip due to self-heating on the PCB. This was identified through coanalysis of the board power tool and system thermal tool.

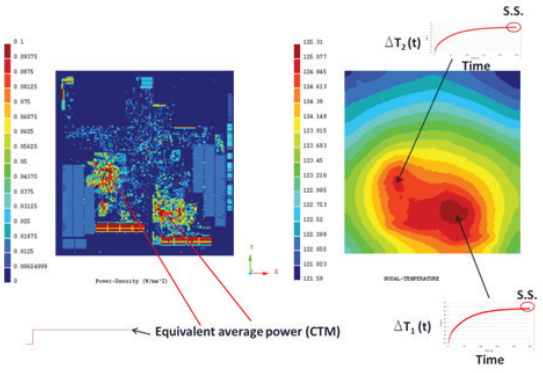

Figure 23. Temperature buildup on chip after power map is switched on

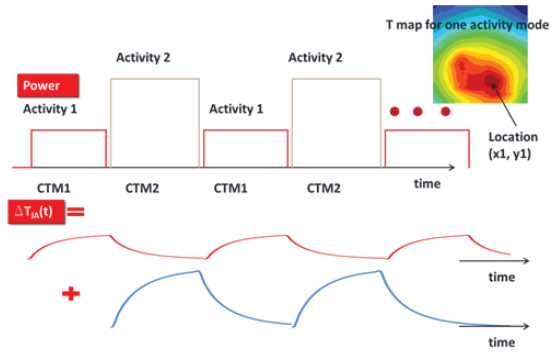

Figure 24. Temporal combination of activities and thermal transients

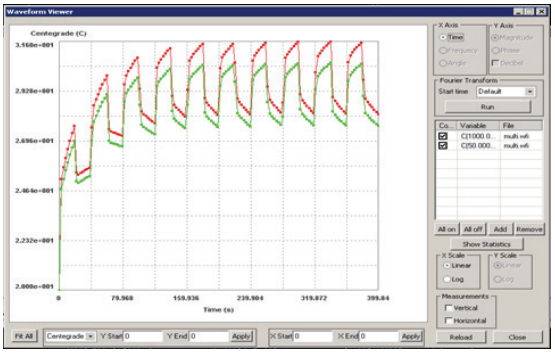

Figure 25. Transient responses at two locations on chip due to two power activities (CTMs) of 10 seconds long each, and repeating 10 times, up to 400 seconds

Conclusion

3-D IC thermal analysis involves tiny features in chips, the package surrounding the chips, and the board or system connecting and surrounding the package. Since they are all thermally coupled, neglecting or oversimplifying one of the components can lead to inaccurate chip temperature prediction. The approach used to cover feature sizes from microns to meters is coanalysis, using tools that are good at managing model sizes in its category. This paper described the key elements in thermal modeling from chip to package to board and system. Typical thermal responses covering chip layers, temperature dependency of chip power, and complex thermal system assembly were presented. A CTM-based thermal analysis is the solution used for integrating the tools at different levels. The converged thermal profile on the chip from the CTM-based thermal analysis is used for temperature-aware EM and IR drop analysis of the chip for design sign-off. Case studies demonstrated 3-D IC package in back annotation to chip, chip–package–system thermal convergence, multiactivity transient responses on chip, and self-heating effects on chip temperature using a thermal co-analysis for 3-D IC chip–package and system.

References

[1] K. Banerjee, M. Pedram, and A. Ajami, Analysis and optimization of thermal issues in high-performance VLSI, ACM/SIGDA International Symposium on Physical Design (ISPD), pages 230-237, April 2001.
[2] S. Im and K. Banerjee, Full chip thermal analysis of planar (2-D) and vertically integrated (3-D) high performance ICs, Tech. Dig. IEDM, 2000, pp. 727-730.
[3] T. Wang, J. Tsai, and C. Chen, “Thermal and Power Integrity based Power/Ground Networks Optimization,” Design, Automation and Test in Europe Conference and Exhibition, 2004.
[4] T. Wang and M. Schmitt, Accurate Thermal Analysis of Chip/Package Systems, http://networksystemsdesignline.com/howto/198001556
[5] T. Song, N. Sturcken, K. Athikulwongse, K. Shepard, and S. K. Lim, Thermal Analysis and Optimization of 2.5-D Integrated Voltage Regulator, EPEPS 2012, pp47~50.
[6] S. Pan, N. Chang, and J. Zheng, et.al. IC-Package Thermal Co-Analysis in 3-D IC Environment, InterPACK2011-52240.
[7] J. Lau, The Most Cost-Effective Integrator (TSV Interposer) for 3D IC Integration System-in-Package (SiP), IPACK2011-52189.
[8] Thermal Integrity of Designs with Silicon Interposer, Apache Redhawk/Sentinel-TI Application Note, TSMC Reference Flow Release 12, June 2011.
[9] Thermal Integrity of 3D IC Designs, Apache Redhawk/Sentinel-TI Application Note, TSMC Reference Flow Release 12, June 2011.
[10] http://en.wikipedia.org/wiki/Integrated_circuit
[11] http://en.wikipedia.org/wiki/Standard_cell
[12] Apache Redhawk user manual
[13] Apache Totem user manual
[14] Apache Sentinel-TI user manual
[15] ANSYS Icepak user manual

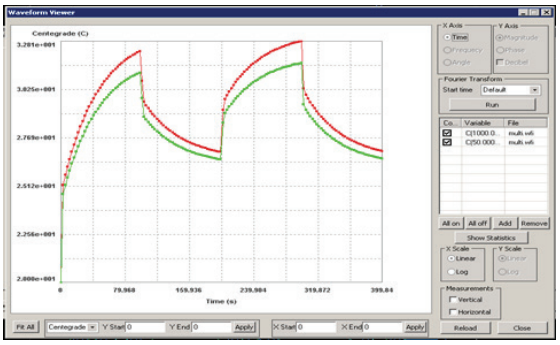

Figure 26. Transient responses at two locations on chip due to two power activities (CTMs) of 100 seconds long each, and repeating twice, up to 400 seconds

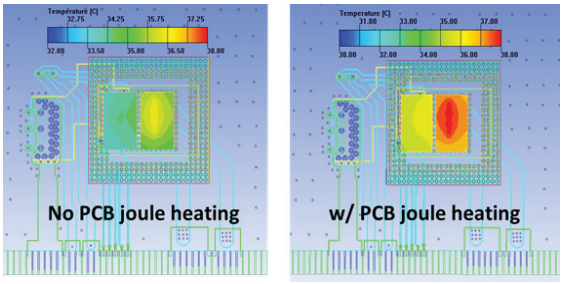

Figure 27. Joule heating or self-heating on a board affects chip temperature.

[16] ANSYS SIwave user manual

[17] J. Adam Butts and Guri Sohi, A Static Power Model for Architects, 33rd International Symposium on Microarchitecture, December 2000

[18] Weste and Eshraghian, Principles of CMOS VLSI Design : a systems perspective, Second Edition, (1993) pp.48 ISBN 0-201-53376-6

[19] Application Note: Chip-Package-System Power and Thermal Co-Analysis with Ansys Tools, TSMC Reference Flow CoWoS, Oct. 2012.

ANSYS, Inc.
Southpointe
275 Technology Drive
Canonsburg, PA 15317
U.S.A.
724.746.3304
ansysinfo@ansys.com

ANSYS, Inc. is one of the world's leading engineering simulation software providers. Its technology has enabled customers to predict with accuracy that their product designs will thrive in the real world. The company offers a common platform of fully integrated multiphysics software tools designed to optimize product development processes for a wide range of industries, including aerospace, automotive, civil engineering, consumer products, chemical process, electronics, environmental, healthcare, marine, power, sports and others. Applied to design concept, final-stage testing, validation and trouble-shooting existing designs, software from ANSYS can significantly speed design and development times, reduce costs, and provide insight and understanding into product and process performance. Visit www.ansys.com for more information.